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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,123	LEE, HOI-JIN	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☒ Claim(s) *16,19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/03, 4/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-25 are presented for examination.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

2. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 119(a)-(d) as follows: The applicant has not filed an English language translation of the document.

3. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

Information Disclosure Statement

4. The examiner has considered the applicant's Information Disclosure Statements dated 11/25/2003 and 4/19/2005.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, as per Claim 16, "receiving the signal from a core circuit on the chip via a plurality of

signal input/output pins" must be shown or the feature canceled from the claim. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities:

Page 6 line 1 should be corrected to read, "... signals and outputting an inverted signal, and/or ...".

Page 6 line 3 should be corrected to read, "... at least one or an odd number of the unit delay circuits ...".

Page 6 paragraph [20] line 8 should be corrected to read, "... approximately ~~1:2:3:5~~ 1N:2N:3N:5N when N may be ...".

Page 6 paragraph [20] line 10 should be corrected to read, "... so long as the ~~for~~ numbers are different ~~form~~ from each other.".

Appropriate correction is required.

Claim Objections

7. Claim 16 is objected to because of the following informalities:

The 1st line should be corrected to read, "... receiving the signal ~~form~~ from a ...".

8. Claim 19 is objected to because of the following informalities:

The 3rd line should be corrected to read, "... plurality of ~~each~~ pads connected ...".

9. Claims 24 and 25 are objected to because the examiner is not sure if the applicant would like the claims to be independent or dependent claims. The applicant is requested to amend the claims to more clearly indicate the type of claims being recited, and to respond to this objection by stating for the record whether the claims are independent or dependent. In the case if the claims are independent, the applicant will be required to submit the appropriate fees.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim limits receiving the signal of Claim 15 from a core circuit on the chip via a plurality of signal input/output pins". The examiner is unsure of how one signal (of Claim 15) can be received via several pins, therefore the claim in it's present form is indefinite.

11. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim limitation, "... using a plurality of each pad ..." is indefinite, and the examiner is not sure what the applicant intends to claim (see objection to same claim). The examiner is unsure of how a plurality of pads can be connected to one output terminal, therefore the claim in it's present form is indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-2, 5-9, 12-21 and 24-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoshita et al. (herein Inoshita), U.S. Patent No. 6477115.

As per Claim 1:

Inoshita teaches a speed binning test circuit, comprising: a plurality of circuit groups (for example FIG.14 and column 15 lines 27-30) arranged along a boundary of a chip circuit (see FIG.1 and column 15 lines 18-26), each circuit group including a different number of unit delay circuits (column 15 lines 27-30); and a plurality of pads (for example, FIG.14 TAP1-3), each pad arranged so that at least one output terminal of unit delay circuits (FIG.14 32a) of the plurality of circuit groups is connected to each of the pads (FIG.14 TAP1), respectively (FIG.14 32a-c).

As per Claims 2, 9 and 18:

Inoshita further discloses the speed binning test circuit, semiconductor device, and method of claim 1, 8 and 15 wherein the plurality of circuit groups include: a first speed correlation circuit (FIG.14 between 12 and 31a) in which unit delay circuits of a first group (the groups are different as per column 15 lines27-30) are serially-connected to one another (column 6 lines 16-28) for delaying a received final delay signal (in the case of ring set-up of FIG.20 applied

to FIG.14, FIG.14 16 is connected to 14) and outputting a first delay signal (FIG.14 TAP1); a second speed correlation circuit (FIG.14 between 31a and 31b) in which unit delay circuits of a second group (the groups are different as per column 15 lines27-30) are serially-connected to one another (column 6 lines 16-28) for delaying the first delay signal and outputting a second delay signal (FIG.14 TAP2); a third speed correlation circuit (FIG.14 between 31b and 31c) in which unit delay circuits of a third group (the groups are different as per column 15 lines27-30) are serially-connected to one another (column 6 lines 16-28) for delaying the second delay signal and outputting a third delay signal (FIG.14 TAP3); and a fourth speed correlation circuit (FIG.14 between 31c and 16) in which unit delay circuits of a fourth group (the groups are different as per column 15 lines27-30) are serially-connected to one another (column 6 lines 16-28) for delaying the third delay signal and outputting the final delay signal (FIG.14 OUT) that is received by the first group of unit delay circuits (as per FIG.20).

As per Claims 5 and 12 and 20:

Inoshita further discloses the speed binning test circuit and semiconductor device and method of claims 2 and 9 and 19, wherein the first through third delay signals, collectively, and the final delay signal have the same oscillation waveforms after a given time (FIG.20 as applied to FIG.14, column 1 lines 60-67 and column 2 lines 1-2).

As per Claims 6 and 13 and 21:

Inoshita further discloses the speed binning test circuit and semiconductor device and method of claims 5 and 12 and 20, wherein the given time represents

a total signal delay time of a signal delayed through the first through fourth groups. (FIG.20 as applied to FIG.14, column 1 lines 60-67 and column 2 lines 1-2).

As per Claim 7:

Inoshita further teaches the speed binning test circuit of claim 1, wherein the unit delay circuits are inverter circuits (see FIG.14).

As per Claim 8:

Inoshita teaches a semiconductor device, comprising: a plurality of signal input/output pins (for example, FIG.21 66); a core circuit (FIG.21 61) including logic that receives or outputs a signal via the plurality of signal input/output pins (column 2 lines 3-11); and a speed binning test circuit composed of a plurality of circuit groups (for example FIG.14 and column 15 lines 27-30), each circuit group including a different number of unit delay circuits (column 15 lines 27-30) arranged in a chain structure (see FIG.14 and column 15 lines 31-33) along the boundary of the core circuit (see FIG.1 and column 15 lines 18-26).

As per Claim 14:

Inoshita further teaches the semiconductor device of claim 8, wherein the unit delay circuits are inverter circuits (see FIG.14).

As per Claims 15, 24 and 25:

Inoshita teaches a speed binning test method based on a semiconductor device containing a test circuit, comprising therein: delaying a signal through a plurality of successively connected circuit groups that forms a chain structure on a chip, and monitoring on-chip-variations (fourth embodiment, column 11 lines

47-62) to determine total signal delay time through the chain structure (applying first and third embodiments, reference column 11 lines 20-47).

As per Claim 16:

Inoshita further teaches the method of claim 15, further comprising receiving the signal from a core circuit on the chip via a plurality of signal input/output pins. In view of the indefiniteness of this claim, the examiner cites Inoshita column 2 lines 3-12, where the signal passes through a delay circuit located in the core and is connected to I/O pads (see FIG.21 63 and 64).

As per Claim 17:

Inoshita further teaches the method of claim 15, wherein each group includes a different number of serially-connected unit delay circuits (see column 15 lines 27-30).

As per Claim 19:

Inoshita further teaches the method of claim 18, wherein the monitoring step further includes monitoring on-chip variations by measuring oscillation waveforms using a plurality of each pad connected to at least one output terminal of unit delay circuit of the circuit groups, respectively that form the chain structure (column 1 lines 60-67 and column 2 lines 1-2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to

be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3-4, 10-11 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoshita et al. (herein Inoshita), U.S. Patent No. 6477115 as applied to Claims 1,8 and 15, in view of Patrie et al. (herein Patrie), U.S. Patent No. 6219305.

As per Claims 3 and10 and 22:

Patrie further discloses that which Inoshita fails to teach, specifically, the speed binning test circuit and semiconductor device and method of claims 1 and 8 and 15, wherein the ratio of numbers of unit delay circuits of the plurality of circuit groups (where in Patrie, the groups are arranged in FIG.11 as shown) are expressed by: A:B:C:D=a:b:c:d. (In regard to Patrie, the disclosure at column 12 lines 43-57 discusses using four delay groups of different sizes in order to minimize effects of clocks on delay measurements. The delay groups of Patrie relate to the delay groups of Inoshita, and thus suggest to Inoshita that more accurate measurements would be attainable when the different groups are arranged in Inoshita using the relationship of Patrie.) Further in regard to the rejection of Claim 1, wherein A denotes a number obtained by subtracting 1 from the numbers of unit delay circuits of a first group (FIG.11 1150, 1145); B denotes the number of unit delay circuits of a second group (FIG.11 1150, 1145, 1140); C denotes the number of unit delay circuits of a third group (FIG.11 1150, 1145, 1135); D denotes a number of unit delay circuits of the fourth group (FIG.11 1150, 1145, 1130), and wherein a, b, c, and d represent different valued

coefficients (1, 3, 5, 7). And in view of the motivation previously stated, the claim is rejected. And Patrie, in column 2 lines 33-35, cites the advantage of a more accurate means for characterizing IC speed performance. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to incorporate the more accurate means of measuring circuit delay of Patrie into the measurement system of Inoshita in order to perform circuit delay measurements with the most accurate results.

As per Claims 4 and 11 and 23:

Patrie further discloses that which Inoshita fails to teach, specifically, the speed binning test circuit and semiconductor device and method of claim 3 and 10 and 22, wherein a, b, c, and d (1, 3, 5, 7) are different prime numbers. And in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

jpt

HEBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100